IN THE CLAIMS

Please amend the claims as follows.

1-76. (Cancelled)

77. (Currently Amended) A vertical memory cell, comprising:

a substantially planar surface;

~~an access device including a mesa, the mesa formed partly within an annular depression and extending outwardly from the planar surface~~;

a first ~~and a second~~ insulator ~~forming a portion of the annular depression~~ adjacent the planar surface,

a second insulator spaced apart from the first insulator, wherein an annular depression is formed in the first insulator and the second insulator;

an access device including a mesa, the mesa formed partly within the annular depression and extending outwardly from the planar surface;

a buried conductive path bounded by the first insulator and [[a]] the second insulator, the buried conductive path enclosing a section of the mesa, the mesa circumferentially contacting the buried conductive path at a specified radius along a vertical sidewall region of the mesa above the first insulator, wherein a portion of the mesa extending radially inward from the buried conductive path and extending vertically along the buried conductive path between the first insulator and the second insulator consists essentially of dopant atoms of one conductivity type, and wherein the dopant atoms in the portion form with a diffused concentration profile in the radial direction; and

a storage device on the mesa.

78. (Previously Presented) The memory cell of claim 77, wherein the first and the second insulators are configured to permit current in the buried conductive path to flow into the mesa only across the specified radius.

79. (Previously Presented) The memory cell of claim 77, wherein the annular depression is formed with a uniform radius.

80. (Previously Presented) The memory cell of claim 77, wherein the annular depression is formed having the specified radius.

81. (Previously Presented) The memory cell of claim 77, wherein the buried conductive path contacts the mesa along the circumference only between the first and the second insulators.

82. (Previously Presented) The memory cell of claim 77, wherein the buried conductive path is a bit line conductor.

83. (Currently Amended) The memory cell of claim 77, wherein the mesa electrically contacts the buried conductive path only ~~at the specified radius~~ along the vertical sidewall region above the first insulator.

84. (Previously Presented) The memory cell of claim 77, wherein the mesa includes a diffused dopant concentration profile in a vertical region configured to contact the storage device.

85. (Currently Amended) A vertical memory cell, comprising:

a substantially planar surface;

~~an access device including a mesa, the mesa formed partly within an annular recess and extending outwardly from the planar surface;~~

a first ~~and a second~~ insulator adjacent the planar surface ~~used to form a portion of the annular recess~~;

a second insulator spaced apart from the first insulator, wherein the first insulator and the second insulator are used to form a portion of the annular recess;

an access device including a mesa, the mesa formed partly within the annular recess and extending outwardly from the planar surface;

a buried conductive path confined by the first insulator and the second insulator, the buried conductive path enclosing a section of the mesa, the mesa circumferentially contacting the buried conductive path at a specified radius along a vertical sidewall region of the mesa above the first insulator, wherein a portion of the mesa extending radially inward from the buried conductive path and extending vertically along the buried conductive path between the first insulator and the second insulator consists essentially of dopant atoms of one conductivity type, and wherein the dopant atoms in the portion arrange in an abrupt concentration profile in the radial direction; and

a storage device on the mesa.

86. (Previously Presented) The memory cell of claim 85, wherein the first and the second insulators are configured to permit a voltage transmitted along in the buried conductive path to couple to the mesa only at the specified radius.

87. (Previously Presented) The memory cell of claim 85, wherein the annular recess is formed with a specified radius.

88. (Previously Presented) The memory cell of claim 85, wherein the annular recess is formed having the specified radius.

89. (Previously Presented) The memory cell of claim 85, wherein the buried conductive path contacts the mesa only along the circumference between the first and the second insulators.

90. (Previously Presented) The memory cell of claim 85, wherein the buried conductive path is a bit line conductor.

91. (Currently Amended) The memory cell of claim 85, wherein the mesa is configured to electrically contact the buried conductive path only ~~at the specified radius~~ along the vertical sidewall region above the first insulator.

92-110. (Cancelled)